WHAT IS CLAIMED IS:

1. A signal processing circuit, comprising:

a decision feedback equalizer for waveform-equalizing a digital signal in accordance with a clock signal and generating the waveform-equalized digital signal; and

a timing recovery PLL, connected to the decision feedback equalizer, for generating the clock signal, the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on the phase difference between the digital signal and the clock signal, and supplying the clock signal to the decision feedback equalizer, wherein the decision feedback equalizer includes,

a prefilter for filtering the digital signal and generating a filtered digital signal,

a decision circuit, connected to the prefilter, for adding a feedback signal and the filtered digital signal and generating an addition signal, and for analyzing the addition signal in accordance with predetermined criteria to generate a decision signal,

a shift register, connected to the decision circuit, for sampling the decision signal in accordance with the clock signal and storing sampling data, wherein the sampling data stored in the shift register is output from the shift register as the waveform-equalized digital signal,

a feedback filter, connected to the shift register, for receiving the sampling data and generating the feedback signal using the sampling data, and

a loop control circuit for monitoring the filtered digital signal and the feedback signal and controlling a feedback loop formed by the decision circuit, the shift register, and the feedback filter based on a monitoring result.

2. The signal processing circuit of claim 1, wherein the loop control circuit generates a control signal for controlling the feedback loop, and the signal processing circuit further comprising a switch, connected between the feedback filter and the decision circuit, responsive to the control signal.

3. The signal processing circuit of claim 1, wherein the loop control circuit calculates an error between the filtered signal and the feedback signal and controls the feedback loop when the error is within a predetermined range at a specific preset control point of the waveform-equalized digital signal.

4. The signal processing circuit of claim 3, further comprising a detection circuit, connected between the decision circuit and the timing recovery PLL, for detecting the phase difference between the decision signal and the clock signal and supplying the detected phase difference to the timing recovery PLL as the phase difference between the digital signal and the clock signal.

5. The signal processing circuit of claim 4, wherein the detection circuit has a plurality of phase comparison gains, and the loop control circuit supplies a control signal to the detection circuit to change the phase comparison gains based on the monitoring result.

6. The signal processing circuit of claim 4, wherein the loop control circuit generates a control signal for controlling the phase difference detected by the detection circuit based on the monitoring result, the detection circuit receives first and second reference signals and the decision signal and supplies the difference between one of the first and second reference signal and the decision signal to the

timing recovery PLL as the phase difference in accordance with the control signal, the first reference signal has a first predetermined value at the preset control point of the filtered digital signal, and the second reference signal has a second predetermined value at the preset control point of the decision signal.

7. The signal processing circuit of claim 3, wherein the loop control circuit includes:

an adder, connected to the prefilter and the feedback filter, for receiving the filtered digital signal and the feedback signal and calculating the error between the filtered digital signal and the feedback signal; and

a comparator, connected to the adder, receiving the error from the adder, comparing the error and a value having a predetermined range, and controlling the feedback loop based on the comparison result.

8. The signal processing circuit of claim 7, wherein the comparator prestores minimum and maximum values defining the predetermined range.

9. In a signal processor, a feedback control method comprising the steps of:

filtering a digital signal to generate a filtered digital signal;

adding a feedback signal and the filtered digital signal to generate the addition signal;

analyzing the addition signal in accordance with predetermined criteria to generate a decision signal;

sampling the decision signal in accordance with a clock signal to store sampling data in a shift register;

generating the feedback signal using the sampling data stored in the shift register;

generating the clock signal, which is substantially coincident with the phase of the digital signal, based on a phase difference between the digital signal and the clock signal;

monitoring the filtered digital signal and the feedback signal; and

selecting whether the feedback signal is fed back to the step of generating the addition signal based on a monitoring result.

10. The method of claim 9, wherein the step of selecting the feedback includes the steps of:

calculating an error between the filtered digital signal and the feedback signal; and

executing the feedback step when the error is within a predetermined range at a specific preset control point of the sampling data.

11. The method of claim 10, wherein the step of selecting the feedback further includes the step of defining the predetermined range using a minimum value and a maximum value.

12. The method of claim 9, further comprising the step of detecting the phase difference between the decision signal and the clock signal, and wherein the step of generating the clock signal includes generating the clock signal substantially coincident with the phase of the digital signal, based on the detected phase difference.

13. The method of claim 12, wherein the step of detecting the phase difference includes detecting the phase difference between the decision signal and the clock signal using a plurality of phase comparison gains, and the method

further comprises the step of determining one of the plurality of phase comparison gains based on the monitoring result.

14. The method of claim 12, wherein the step of detecting the phase difference includes detecting the difference between one of a first or second reference signal and the decision signal as the phase difference, the first reference signal has a first predetermined value at the preset control point of the filtered digital signal, and the second reference signal has a second predetermined value at the preset control point of the decision signal, and the method further comprises the step of selecting one of the first and second reference signals based on the monitoring result.

15. In a signal processor, a feedback control method comprising the steps of:

filtering a digital signal to generate a filtered digital signal;

adding a feedback signal and the filtered digital signal to generate the addition signal;

analyzing the addition signal in accordance with predetermined criteria to generate a decision signal;

sampling the decision signal in accordance with a clock signal to store sampling data in a shift register;

generating the feedback signal using the sampling data stored in the shift register;

calculating a first phase difference between the digital signal and the clock signal using the decision signal and a first reference signal, wherein the first reference signal has a first predetermined value at preset control point of the filtered digital signal;

generating the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on a first phase difference;

determining whether the first phase difference is within a predetermined range;

feeding back the feedback signal to the step of generating the addition signal when the first phase difference is within the predetermined range;

calculating a second phase difference between the digital signal and the clock signal using the decision signal and a second reference signal, wherein the second reference signal has a second predetermined value at the preset control point preset of the decision signal; and

regenerating the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on the second phase difference.